What is claimed is:

1. A data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program, comprising

an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory,

a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide, and

a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and performing processing according to the read instruction codes when said coincidence signal is output by said comparison means.

2. A data processing apparatus as set forth in claim 1, wherein said comparison means comprises an interrupt request means for outputting an interrupt

request signal as said coincidence signal when a program address coincides with the bug address held in the address holding means.

3. A data processing apparatus as set forth in claim 2, wherein the apparatus further comprises

a rewritable memory for storing a debugging program input from the outside during initialization and

an interrupt vector for storing a start address of a memory area storing said debugged program.

4. A data processing apparatus as set forth in claim 3, wherein said program executing means comprises an interrupt processing means for suspending an instruction being executed when receiving said interrupt request signal, reading said debugging program from the address designated by said interrupt vector, and performing processing accordingly.

5. A data processing apparatus as set forth in claim 4, wherein said interrupt processing means sets a return address for returning to the suspended program after the interrupt processing according to an address stored at the end of said debugging program after execution of said debugging program.

6. A data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program,

comprising

a plurality of basic units each including

an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory and

a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide,

the number of basic units corresponding to the number of bugs included in the program, and

a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and performing processing according to the read instruction codes when said coincidence signal is output by any one of said comparison means.

7. A data processing apparatus as set forth in claim 6, wherein said comparison means comprises an interrupt request means for outputting an interrupt

request signal as said coincidence signal when a program address coincides with the bug address held in the address holding means.

8. A data processing apparatus as set forth in claim 7, further comprising

a writeable memory for storing a debugging program input from the outside during initialization and

an interrupt vector for storing the start address of a memory area storing said debugging program.

9. A data processing apparatus as set forth in claim 8, wherein said program executing means comprises an interrupt processing means for suspending an instruction being executed when receiving said interrupt request signal, reading said debugging program from the address designated by said interrupt vector, and performing processing accordingly.

10. A data processing apparatus as set forth in claim 9, wherein said interrupt processing means comprises

an interruption recording means for recording the number of interruptions and

a branch means for branching to a predetermined debugging program among a plurality of the debugging programs stored in the memory according to the number of interruptions recorded by the interruption times

recording means.

11. A data processing apparatus as set forth in claim 9, wherein an address to be returned to when returning to the original program when the debugging program is finished is stored at the end of each debugging program, and said interrupt processing means sets a return address for returning to the original program after the execution of any of the debugging programs according to the return address stored at the end of the debugging program.

12. A data processing apparatus as set forth in claim 10, wherein said interruption recording means is a memory of a predetermined address in the rewritable memory storing the debugging programs and wherein the content of the memory is rewritten by said interrupt processing means.